Fast page-mode memory eliminates most of the setup time for column addresses within a page, so it is faster and consumes less power than page-mode memory. With fast page-mode memory, memory accesses for an entire page were usually fast enough to reduce wait states in processors available for use with this type of memory. However, when the processor requests data from a different page, both row and column addresses have to be changed, and the resulting delay is similar to ordinary page-mode operation. See "Fast Page Mode (FPM)", Id.

EDO memory is similar to fast page-mode memory in that an entire page of memory can be read very quickly. The major advantage of EDO memory is that it modifies CAS timing to hold data at the chip's output pins longer. This means that the output data can be read while the CAS signal is de-asserted and set up for the next cycle, resulting in less waiting. With EDO memory, data can be read or written (within a page) as fast as the memory chip will accept new column addresses. EDO allows more overlap between column accesses and data transfers than fast page-mode memory, eliminating most of the wait and resulting in a considerable performance improvement. See "Extended Data Output RAM (EDO)", Id.

Burst EDO memory improves EDO performance by adding **a pipeline stage** (i.e., **a pipelined architecture**) to permit reads or writes to occur in four row-address bursts. After the initial page address is applied to a burst EDO chip, the chip typically provides three more sequential addresses (within a page). This address circuitry eliminates the time required to detect and latch externally supplied addresses. However, burst EDO memory including a pipelined architecture does not accept external addresses so as to operate in a pipelined mode (as defined by the Appellants in the Application). See "Burst Extended Data Output RAM (BEDO)", Id.

In some embodiments of the Appellants' invention, a newburst signal from control logic is provided. The newburst signal is fed to a multiplexer for choosing which type of addressing is to occur. For one type of addressing, burst operation is provided beginning with a stored initial external address. A counter is then used to increment the initial external address. (Application, Pg. 29, lines 8-25)

In pipelined mode, address information is divided into operational times. As address information passes through the memory, it is operative in one operational area before moving onto another operational area. However, once moved, another set of address information may

enter the operational area exited. Thus, by time slicing address information, accesses to a memory may overlap without conflicting. This allows for a continuous data stream of address information in the form of external addresses. Therefore, **internal addresses are not generated in pipelined mode**. Rather, addresses are provided from an external source as a stream of data. In page mode, with one enable signal held active and another enable signal cycled, an external address is received on each cycle of the cycled enable signal. For example, if /RAS is held active, and /CAS is cycled, a random or determined order of columns associated with the row address may be accessed in pipelined mode, whereas in burst mode, a predetermined pattern of columns may be accessed. (Application, Pg. 8, lines 1-13)

In short, what is discussed by Manning is not identical to the subject matter of the present invention as required by the M.P.E.P., and therefore, the rejection under § 102 is improper. Reconsideration and allowance of claims 36-39, 59-64, 69, and 75-83 is respectfully requested.

c.2 **-- The rejection under § 103**

Claims 65-68 were rejected under 35 USC § 103(a) as being unpatentable over Manning in view of Rosich. First, the Appellants do not admit that Manning or Rosich are prior art and reserve the right to swear behind these references in the future. Second, since each of the references fail to teach the element of *switching, selecting, or choosing* between pipelined and burst modes of operation, since the proposed combination of references would be inoperative, and since the references teach away from such a combination, the Appellants respectfully traverse this rejection under § 103 by the Office.

The Appellants are unable to find how combining Manning with Rosich serves to teach the invention disclosed in claims 65-68. The Appellants have already discussed why Manning is defective as a reference (i.e., Manning does not disclose *selecting, choosing, or switching* between burst and pipelined modes of operation). Even so, many assertions are made in various Office Actions respecting the instant Application to the effect that Manning discloses switching or changing modes to a pipelined mode (even to the extent of specifying where in the cycles of a memory operation the change to a pipelined mode occurs (see § 9 of the Office Action mailed to the Appellants on 3/15/02, regarding claims 66-67). However, the Appellants can find no such teaching in Manning. No reply has been received by the Appellants in response to several

requests for more specific citations to how such activity is enabled by the references. Instead the single statement in Manning (col. 5, lines 43-50) which alludes to the possible existence of a pipelined architecture has been repeatedly presented by the Office. This text provides no description as to how the architecture would be implemented, especially with regard to changing between a pipelined mode and other operational modes at will, in the same memory, using individual operational signals, as occurs in some of the embodiments disclosed by the Appellants. As explained above, this is because the term "pipelined architecture" refers to pipelined registers used for the rapid generation of *internal* addresses in burst EDO memory.

In rejecting claim 65, the Office Action states: "Rosich discloses the step of changing the mode select signal to select a mode of operation while maintaining a first enabling signal in an active state ... (... RASL in Fig. 7)". From this statement, it is apparent that the RAS L signal of Rosich is being interpreted in the Office Action as the "first enabling signal" of claim 65. Thus, the Office Action relies on Rosich to teach switching modes of operation while maintaining the RAS L signal in the active state. However, it should be noted that Rosich specifically states "... the DRAM **will not change from page mode to nibble mode** until the next assertion of the CAS signal after the assertion of the RAS signal." See Rosich et al., Col. 9, lines 6-9. In other words, until the RAS signal as been re-asserted (not "maintained", as claimed by the Appellants), changing operational modes is not possible.

Further support for this operational requirement of the device disclosed by Rosich can be found by referring to FIG. 5A of Rosich. If WE L is not asserted (i.e., is high, indicating a read) on the first assertion of CAS L following the assertion of RAS L, the counter enable (CEN) signal will be high, and the DRAM will be configured for nibble mode. If, on the other hand, WE L is asserted (i.e., is low, indicating a write) on the first assertion of CAS L following an assertion of RAS L, CEN will be low, and the DRAM will be configured for page mode. In either case, after the DRAM configuration has been selected following assertion of the RAS L signal, the configuration cannot be switched until after the RAS L signal is deasserted (clearing flip-flops 540 and 550 in FIG. 5A). This is consistent with the specification in Rosich, which states "The DRAM will **remain in nibble mode until RAS is deasserted** resetting the outputs of flip-flop 550". See Rosich et al., Col. 8 lines 49-50. Thus, once the DRAM is configured for

either the nibble mode or page mode following an assertion of RAS L, the DRAM will *remain in that mode* until after the RAS L signal is deasserted and then asserted again.

Therefore, the Office Action assertion that Rosich discloses switching modes of operation while maintaining the RAS L signal in active state is erroneous, and it is respectfully submitted that the Office Action has failed to make out a *prima facie* case of obviousness at least because the cited references do not show or suggest "changing the mode select signal to select a pipeline mode while maintaining a first enabling signal in an active state", as recited in claim 65.

Rosich merely discloses switching between a page mode and a nibble mode. There is no discussion of a pipelined access mode by Rosich, whatsoever. Thus, the combination of Rosich with Manning does not cure the admitted primary defect of Manning, nor the failure of each of the cited references to disclose switching between burst and pipelined modes of operation.

The assertion has been made in the Office Action that "one of ordinary skill in the art ... would have recognized that the memory access cycle of Manning would have been reduced by maintaining a first enable signal in an active state during mode [sic] of operations because it would provide a capability of that the memory is always in ready [sic] to receive a mode command thereby increasing the access speed of the memory. Increasing memory speed would have a highly desirable feature in the computer system environment of Rosich because the objective of computer system [sic] is increasing speed or computing power. Therefore, it would have been obvious to incorporate the step of maintaining a first enabling signal in [sic] active state of Rosich in Manning because it would increase memory access speed of Manning by providing a capability of that the memory is always in [sic] ready to receive a command." However, as demonstrated above, maintaining the state of the RAS L signal *prohibits* changing modes. Thus, there is no evidence in the record as to why it would be obvious to incorporate Rosich's RAS L signal into the operation of Manning to provide *a single memory device which selectably operates in both burst and pipelined modes*, as occurs in some embodiments disclosed by the Appellants. This complete absence of evidence in the record fails to satisfy the explicit requirements set forth by the *In re Sang Su Lee* court. Thus, the Examiner appears to be using personal knowledge to support this combination of references, and is again respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

Finally, Rosich teaches away from the combination urged by the Office Action because, as has already been demonstrated, Rosich's RAS L signal *can not* be maintained while mode changes are effected. The M.P.E.P. requires that any asserted combination of references must not render the prior art unsatisfactory for its intended purpose, or change the principle of operation of the reference being modified. *See* M.P.E.P. § 2143.01. One of ordinary skill in the art would not be led to change modes in the device of Manning by using an inoperable mechanism of Rosich. Such modification would render the apparatus of Manning unfit for its intended purpose.

Since the page/nibble mode DRAM of Rosich, as well as the EDO memory of Manning do not include each of the elements claimed by the Appellants, since there is no evidence in the record supporting a motivation to combine the references, and finally, since the references teach away from such a combination, the Appellants respectfully request reconsideration and withdrawal of the rejection of claims 65-68 under 35 U.S.C. §103.

c.3 Why the claims are separately patentable:

While the separate patentability of each claim has been discussed in the "argument" section above, as allowed in the M.P.E.P. § 1206, the reasons are summarized here to ensure completeness and as a matter of convenience for the Board.

Independent claim 36 includes "selecting between a burst mode and a pipelined mode of operation of ... [an] asynchronously accessible DRAM". Dependent claims 37-39 refine this concept by including the limitations on the order of address access "in the pipelined mode" (claims 37), or "in the burst mode" in conjunction with selecting between the burst and pipelined modes of operation (claim 38); and "selecting at least one address pathway based on the selection between the burst mode and the pipelined mode" (claim 39). Neither Manning nor Rosich, nor any proper combination of these references discloses these elements. None of these limitations depends on the other, and each dependent claim is separately patentable from the other, and from independent claim 36.

Independent claim 59 includes the element of "choosing whether the memory is in a burst mode ... or in a pipeline mode of operation". Dependent claims 60-62 add the limitations of "switching between the burst mode ... and the pipelined mode", "switching between ... read ... and write operation[s]" in conjunction with choosing a pipelined mode of operation, and

"operations ... performed in a different order" in conjunction with choosing a pipelined mode of operation. Neither Manning nor Rosich, nor any proper combination of these references discloses these elements. None of these limitations depends on the other, and each dependent claim is separately patentable from the other, and from independent claim 59.

Independent claim 63 includes "selecting an external address only data path ... if ... the pipelined mode of operation is selected" and "receiving an external row address". Dependent claim 64 adds the further limitation of "operations ... performed in a different order" (including selecting a pipelined mode of operation). Neither Manning nor Rosich, nor any proper combination of these references discloses these elements. None of these limitations depends on the other, and each dependent claim is separately patentable from the other, as well as from the independent claims.

Independent claim 65 and 67 include "changing [a] ... mode select signal to select a pipelined mode of operation", while dependent claim 66 adds the limitation of "switching the mode of operation to a pipelined mode". Independent claim 65 includes the additional limitation of "receiving a mode select signal". Neither Manning nor Rosich, nor any proper combination of these references discloses these elements. None of these limitations depends on the other, and each dependent claim is separately patentable from the other.

Independent claim 68 includes "selecting an external address only data path ... when the pipelined mode of operation is selected." Neither Manning nor Rosich, nor any proper combination of these references discloses these elements. This independent apparatus claim is separately patentable from all of the other claims.

Independent claim 69 describes a storage device including mode circuitry "configured to select between a burst mode and a pipeline mode" along with "an external column address data path for pipeline read and write operation column address retrieval". Neither Manning nor Rosich, nor any proper combination of these references discloses these elements. This independent apparatus claim is separately patentable from all of the other claims.

Independent method claims 75 and 80 include the element of "switching from a burst mode ... to a pipelined mode", while dependent claims 77 and 82 add the limitation of "selecting at least one address pathway" based upon such switching. Dependent claims 78 and 83 add the

limitation of "subsequently switching from the pipelined mode ... to the burst mode". Dependent claim 79 adds the limitation of "selecting at least one address pathway" based upon such subsequent switching. Independent claim 75 adds the possiblity of "selecting a ... write operation." Neither Manning nor Rosich, nor any proper combination of these references discloses these elements. None of these limitations depends on the other, and each dependent claim is separately patentable from the other, as well as from the independent claims.

c.4 Double patenting rejection:

Claim 66 was provisionally rejected under the judicially created doctrine of double patenting over claims 51, 59, 63, 64, and 67 of co-pending Application No. 08/984,561, presently allowed. Appellants will consider filing a Terminal Disclaimer to obviate any remaining double patenting rejections upon receipt of an indication that the present claims are otherwise allowable.

9. SUMMARY

It is respectfully submitted that neither has a *prima facie* case of anticipation under 35 U.S.C. §102 been established, nor has a *prima facie* case of obviousness under 35 U.S.C. §103 been established. Reconsideration and withdrawal of the rejections of claims 36-39, 59-69, and 75-83 is therefore respectfully requested. Should the Board be of the opinion that a rejected claim may be allowable in amended form, an explicit statement to that effect is also requested.

The Examiner is invited to telephone Appellants' attorney, Mark Muller, at (210) 308-5677, or the undersigned attorney, to facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

JEFFREY S. MAILLOUX ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 349-9587

Date 14 May 2003 By ______________________

Timothy B. Clise
Reg. No. 40,957

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Gina M. Uphus

Name ______________________ Signature ______________________

APPENDIX I

The Claims on Appeal

36. A method for accessing an asynchronously-accessible dynamic random access memory, comprising:

receiving an external row address to the asynchronously-accessible dynamic random access memory;

selecting between a burst mode and a pipelined mode of operation of the asynchronously-accessible dynamic random access memory;

selecting between a read operation and a write operation of the asynchronously-accessible dynamic random access memory; and

obtaining a first external column address for accessing the asynchronously-accessible dynamic random access memory.

37. The method, as in Claim 36, further comprising:

obtaining a second external column address subsequent to the first external column address for operation in the pipelined mode.

38. The method, as in Claim 36, further comprising:

generating an internal column address subsequent to the first external column address for operation in the burst mode, the internal column address patterned after the first external column address.

39. The method, as in Claim 36, further comprising:

selecting at least one address pathway based on the selection between the burst mode and the pipelined mode.

59. A method of accessing a memory, comprising:

receiving an external row address;

choosing whether the memory is in a burst mode of operation or in a pipeline mode of operation;

selecting a read operation or a write operation for the memory; and

executing a read or write operation in the chosen mode of operation.

60. The method of claim 59, and further comprising:

switching between the burst mode of operation and the pipelined mode of operation.

61. The method of claim 59, and further comprising:

switching between the read operation and the write operation.

62. The method of claim 59, wherein the operations are performed in a different order.

63. A method of accessing a memory, comprising:

receiving an external row address;

selecting a burst mode of operation or a pipeline mode of operation of the memory;

selecting a read operation or a write operation for the memory;

selecting an external address only data path, obtaining an external column address, and obtaining information from the memory if the read operation of the pipeline mode of operation is selected;

selecting an external address only data path, obtaining an external column address, and providing information to the memory if the write operation of the pipeline mode of operation is selected;

selecting an initial buffered external address data path, obtaining an initial external column address, obtaining information from the memory, and generating internal column addresses and obtaining further information from the memory until all desired internal column addresses are used if the read operation of the burst mode of operation is selected; and

selecting an initial buffered external address data path, obtaining an initial external column address, providing information to the memory, and generating internal column addresses and providing further information to the memory until all desired internal column addresses are used if the write operation of the burst mode of operation is selected.

64. The method of claim 63, wherein the operations are performed in a different order.

65. A method of operating a memory circuit, comprising:

receiving a mode select signal;

receiving an initial external address;

selecting a read or a write operation of the memory;

cycling a second enabling signal multiply between active and inactive;

generating an internal address on a cycle of the second enabling signal based on the initial external address;

changing the mode select signal to select a pipeline mode of operation while maintaining a first enabling signal in an active state; and

receiving an external address on each cycle of the second enabling signal.

66. A method for accessing a memory, comprising:

maintaining a first enabling signal in an active state;

maintaining a mode select signal to select a burst mode of operation;

receiving an initial external address;

selecting a read or a write operation of the memory;

cycling a second enabling signal multiply between inactive and active;

generating an internal address on a cycle of the second enabling signal based on the initial external address; and

switching the mode of operation to a pipeline mode on successive cycles of the second enabling signal by changing the mode select signal.

67. A method for operating a memory, comprising:

maintaining a first enabling signal in an active state;

maintaining a mode select signal to select a burst mode of operation;

selecting a read operation or a write operation of the memory;

receiving a stream of addresses and cycling a second enabling signal for processing the stream of addresses; and

changing the mode select signal to select a pipeline mode of operation.

68. A method for data transfer direction selection in a memory, comprising:

selecting a read or a write operation of the memory;

selecting a burst or a pipeline mode of operation for the memory;

selecting an external address only data path, obtaining an external column address, and accessing the memory when the pipeline mode of operation is selected; and

selecting an initial buffered external address data path, obtaining an inital external column address, accessing the memory, and generating internal column addresses when the burst mode of operation is selected.

69. A storage device comprising:

mode circuitry configured to select between a burst mode and a pipelined mode;

selection circuitry for selecting between a read operation and a write operation;

an external column address data path for pipeline read and write operation column address retrieval;

an internal column address generation module for burst read and write operation column address generation; and

pipelined/burst circuitry coupled to the mode selection circuitry and configured to switch between the pipelined mode and the burst mode for operating the storage device in either mode.

75. A method for accessing an asynchronously-accessible dynamic random access memory (DRAM), comprising:

receiving an external row address to the asynchronously-accessible DRAM;

switching from a burst mode of operation to a pipelined mode of operation;

selecting a memory operation selected from a group consisting of a read operation and a write operation; and

obtaining a first external column address for accessing the asynchronously-accessible DRAM.

76. The method of claim 75, further comprising:

obtaining a second external column address subsequent to obtaining the first external column address for operation in the pipelined mode.

77. The method of claim 75, further comprising:

selecting at least one address pathway based on switching to the pipelined mode of operation.

78. The method of claim 75, further comprising:

subsequently switching from the pipelined mode of operation to the burst mode of operation;

generating an internal column address subsequent to the first external column address for operation in the burst mode, the internal column address patterned after the first external column address.

79. The method of claim 78, further comprising:

selecting at least one address pathway based on subsequently switching to the burst mode of operation.

80. A method for accessing an asynchronously-accessible dynamic random access memory (DRAM), comprising:

receiving an external row address to the asynchronously-accessible DRAM;

switching from a burst mode of operation to a pipelined mode of operation;

selecting a memory read operation; and

obtaining a first external column address for accessing the asynchronously-accessible DRAM.

81. The method of claim 80, further comprising:

obtaining a second external column address subsequent to obtaining the first external column address for operation in the pipelined mode.

82. The method of claim 80, further comprising:

selecting at least one address pathway based on switching to the pipelined mode of operation.

83. The method of claim 80, further comprising:

subsequently switching from the pipelined mode of operation to the burst mode of operation; and

generating an internal column address subsequent to the first external column address for operation in the burst mode, the internal column address patterned after the first external column address.

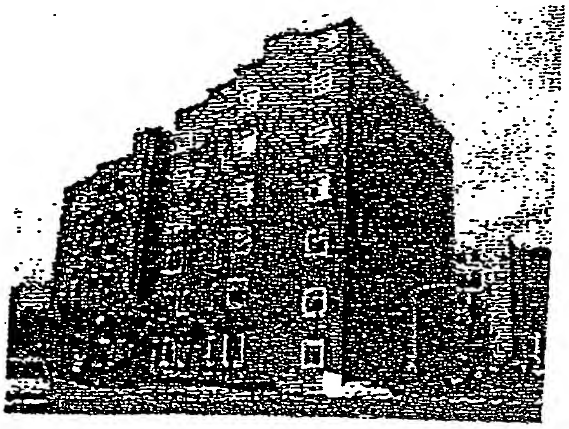
APPENDIX II

Reference

I. Other References

"Burst Extended Data Output RAM (BEDO)", Shuttle Inc., Frequently Asked Questions, December 14, 1999

Company



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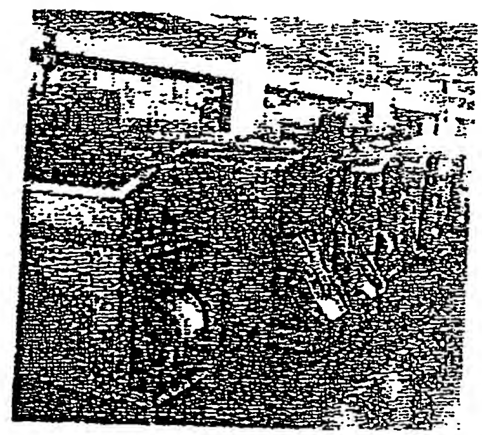

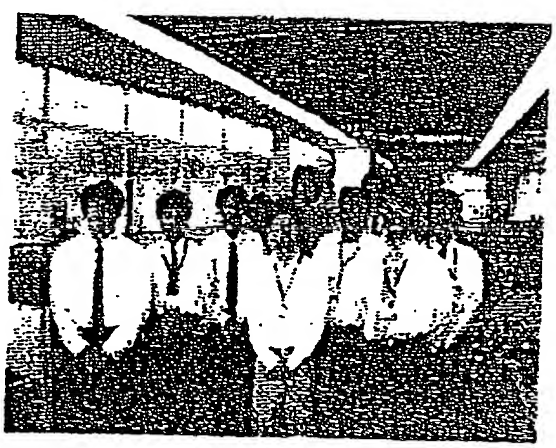

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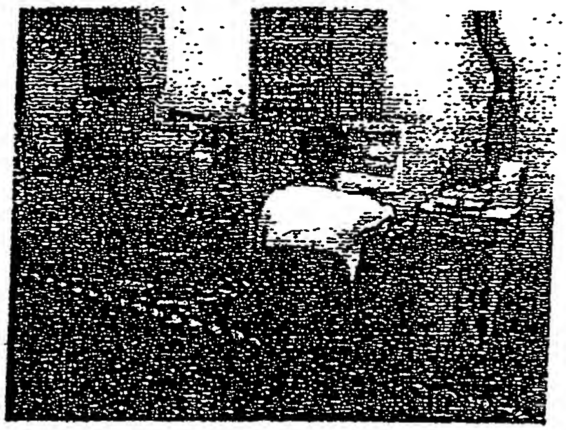

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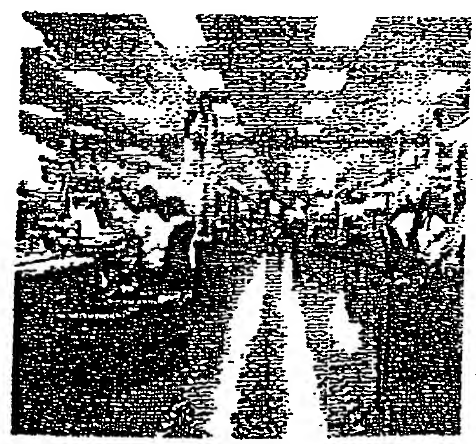

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Frequently Asked Questions

SIMMs and DIMMs

Chapter set below:
SIMMs (Single In Line Memory Modules)
DIMMs (Dual In Line Memory Modules)

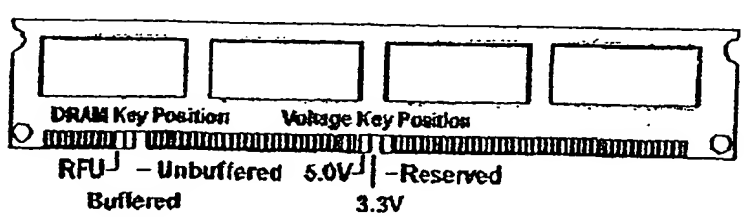
The names SIMM and DIMM only specifies the package RAM comes in, not the type! You can get each RAM type (FPM, EDO, SDRAM,...) for each module, but as fas as PCs are concerned, DIMMs are at present only used for SDRAM.

SIMMs (Single In Line Memory Modules)

SIMMs have 72 Pins and data path width of 32 Bit (36 Bit using Parity-Modules). On Pentium-Mainboards two SIMMs of the same kind and capacity have to be used to fill a bank. Some chipsets (for exp. SIS) allow to use only one module which results in a high performance loss.

DIMMs (Dual In Line Memory Modules)

DIMMs have 168 Pins. The data path width is 64 Bit (72 Bit using Parity-Modules). For this reason you can use a single DIMM to fill a bank on a Pentium-Board. Modules must be 3.3V Unbuffered SDRAM or EDO (you can identify type as shown by the illustration above).



Types of memory (FPM, EDO, SDRAM, ...)

Chapter set below:
Fast Page Mode (FPM)
Extended Data Output RAM (EDO)
Burst Extended Data Output RAM (BEDO)
Synchronous Dynamic RAM (SDRAM)

Fast Page Mode (FPM)

Fast Page Mode are standard memory modules. Actually VRAM or Video RAM is nothing much different, it only is so called dual ported, which means it can be accessed by the

RAMDAC independently of the CPU accesses via the second port, so that the RAMDAC doesn't have to wait for the CPU access to finish. FPM DRAMs for mainboards comes in two different flavors nowadays: 60ns and 70ns access time. On 66 MHz system-clock you should use 60ns modules, however, 70ns work in most cases as well. "Fast Page Mode" means that the module assumes that the next access is in the same memory area (ROW) to speed up the operation. The fastest access in CPU-Cycles is 5-3-3-3 for a data burst of 4 (Byte / Word / Dword).

Extended Data Output RAM (EDO)

The major difference between FPM and EDO is the timing of the CAS#-Signal and Data output using a latch. This speeds up sequential read-operations. The fastest access in CPU-Cycles is 5-2-2-2.

Burst Extended Data Output RAM (BEDO)

In opposition to EDO data latch on BEDO is replaced by a register (i.e. an additional latch stage is added) data will not reach the outputs as a result of the first CAS cycle. The benefit of this internal pipeline stage is that data will appear in a shorter time from the activating CAS edge in the second cycle (i.e. tcas is shorter). The second difference is that BEDO devices include an internal address counter so that only the initial address in a burst of four needs to be provided externally. The fastest access in CPU-Cycles is 5-1-1-1.

Synchronous Dynamic RAM (SDRAM)

As the name says already, this RAM is able to handle all input and output signals synchronized to the system clock - that is something a short while ago only Static Cache RAM was able to achieve. System clock can be higher than 66Mhz. „PC/100"-modules support 100 MHz clock frequency for chipsets with this feature (e.g. Intel 440BX or VIA MVP3). The fastest access in CPU-Cycles is 5-1-1-1 (as fast as BEDO).

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message received from paging device 35 in the data record of Subscriber X in message database 25 (method step 340).

FIGURE 5 is a flow diagram 400 illustrating a wireless message retrieval operation of a representative wireless messaging distribution system in accordance with one embodiment of the present invention. Initially, wireless messaging distribution system 20 receives a connection request from Subscriber X, who is attempting to retrieve and display stored wireless messages (method step 405). Before allowing this transaction, wireless messaging distribution system 20 authenticates the identity of Subscriber X by requesting that Subscriber X enter a Subscriber ID and a corresponding password (method step 410). If the password entered by Subscriber X does not match the stored password, wireless messaging distribution system 20 rejects the connection request from Subscriber X (method steps 415 and 420). If the password entered by Subscriber X matches the stored password for Subscriber X data record in message database 25, wireless messaging distribution system 20 retrieves the data record of Subscriber X from message database 25 (method steps 415 and 425).

Next, wireless messaging distribution system 20 sends selected fields of the stored wireless messages to message retrieval computer 60 used by Subscriber X (method step 430). By sending

only selected portions of the stored wireless messages, rather than the entirety of the stored wireless messages, wireless messaging distribution system 20 allows Subscriber X to review the truncated/abbreviated information before requesting that all of one or more wireless messages be downloaded to message retrieval computer 60. This advantageously conserves bandwidth between wireless messaging distribution system 20 and message retrieval computer 60 and prevents the undesirable downloading of unexpectedly large attached documents to Subscriber X without first warning of the size of the attached document.

After Subscriber X has reviewed the selected wireless message information displayed on message retrieval computer 60, wireless messaging distribution system 20 may receive selected requests from Subscriber X to download complete wireless messages from message database 25 to message retrieval computer 60 (method step 435). Upon receiving such a complete message retrieval request, wireless messaging distribution system 20 sends corresponding complete wireless messages and response/follow-up messages, if any, to message retrieval computer 60 (method step 440).

Finally, wireless messaging distribution system 20 may receive from Subscriber X one or more response/follow-up messages corresponding to one or more of the complete wireless messages and

response/follow-up messages that were downloaded to message retrieval computer 60 (method step 445). Wireless messaging distribution system 20 may then forward the response/follow-up message(s) to the sender(s) of the original wireless message(s) sent to Subscriber X (method step 450).

In a preferred embodiment of the present invention, accessing a message through message retrieval computer 60 before the message has been delivered by RF transmission to a pager may cause the cancellation of the RF transmission if the subscriber chooses that option. For example, if a subscriber has traveled outside of the subscriber's coverage area (or has turned the pager "OFF"), the subscriber may nonetheless use message retrieval computer 60 to retrieve a message that has not been delivered to the pager. When the subscriber returns to the subscriber's coverage area (or turns the pager "ON" again), RF transceiver 30 will transmit what is now a redundant message to the subscriber. To prevent this from happening, the subscriber may select a system option that cancels the subsequent RF transmission of any currently undelivered message if the undelivered message is first retrieved by message retrieval computer 60.

Although the principles of the present invention have been described in detail with reference to message paging system and

infrastructure embodiments, those of ordinary skill in the art should understand that they can make various changes, substitutions and alterations herein without departing from the spirit and scope of the invention in its broadest form.